Controlled, selective III/V nanowire heteroepitaxy

M. Cantoro, G. Brammertz, M. Leys, S. Degroote, M. Heyns, S. De Gendt
IMEC vzw
Kapeldreef 75, 3001 Leuven, Belgium

Abstract

Semiconducting, 1-D nanowires represent an attractive building block when evaluating the progressive scaling of chip dimensions according to the ITRS and the possibility to accommodate more and diverse functionalities on the same platform. Additionally, when III/V semiconductors are tailored into nanowires by adopting bottom-up, CMOS-compatible technology routes, it is also possible to exploit their electronic and optical properties, in many ways superior to those of Si (larger carrier mobilities, direct bandgap option, quantum confinement effects), to realise novel and complex architectures.

In this talk I will focus on the recent advances achieved in the field of heteroepitaxy of III/V nanowire (hetero)structures on lattice-mismatched non-polar semiconducting substrates, putting special emphasis on catalyst-free growth techniques and their relevance for semiconductor industry. Results of selective-area growth experiments will be compared with the existing state-of-the-art. Nanowire structural and electrical characterisation will be presented and the issues more critical for device performance will be reviewed, such as heterointerface quality, extent of lattice defects, degree of control of nanowire orientation with respect to the underlying substrate. Lastly, an outlook on the problem of direct monolithic integration of bottom-up nanowire technology with conventional Si technology will be given.