Epitaxial Graphene Growth on SiC Wafers

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Graphene, a single sheet of sp^2 bonded carbon atoms possessing unique and unusual electrical, mechanical, physical, and chemical properties, has the scientific community searching for samples viable in new technological applications, such as post-CMOS digital electronics and high frequency (>100 GHz) emitters. This search is driving efforts to form epitaxial graphene on large area substrates. To that end, the formation of epitaxial graphene via the thermal desorption process of Si from SiC, pioneered by Berger *et al.* (1), is very attractive since SiC substrates up to 100 mm in diameter are commercially available. We have investigated this approach (2) and have recently synthesized epitaxial graphene with excellent properties on Si-face 50 mm SiC wafers. In this presentation, our progress to achieve wafer-scale epitaxial growth of graphene using a commercial SiC chemical vapor deposition reactor will be described.

Graphene layers were created on C- and Si-face, semi-insulating, on-axis 4H- and 6H-SiC substrates. Semi-insulating substrates were used to facilitate subsequent electrical measurements. An Aixtron VP508 CVD reactor was used as this tool is known to have excellent temperature uniformity for SiC epitaxy at ~1600 °C, which we believe is essential for high quality graphene. A process was developed where the substrates were etched in hydrogen at 1600 °C in order to remove about 300 nm of polishing/wafering damage from the substrate and leave the resulting surface dominated by uniform SiC steps (0.5 nm for Si-face and 1.0 to 1.5 nm for C-face). After etching, graphene epitaxy immediately followed at growth temperatures ranging from 1225 to 1700 °C and pressure $< 10^{-4}$ mbar.

Our investigation initially focused upon growing graphene over a wide range of conditions for both faces and polytypes on intermediate sized (16 x 16 mm^2) samples in order to discern the optimal epitaxy conditions. Significant differences in graphene epitaxy on Si- and C-face samples were found. For example, we noted that X-ray photoelectron spectroscopy found an interfacial C species for growth on the Si-face whereas no interfacial species was observed for growth on C-face. Also, graphene morphology on C-face was markedly different from Si-face epitaxy; the former was dominated by dense arrays of ridges ("giraffe stripes"). Furthermore, images by atomic force microscopy and scanning tunneling microscopy show the giraffe stripes can be found in a wide array of orientations with respect to the step edges. Growth conditions that resulted in high transport mobilities for Si-face samples were high temperatures, > 1500°C, and long times. Growth conditions that yielded good transport values for C-face samples were low temperatures, ≤ 1500°C, and short times. Under these growth conditions, C-face samples are thicker (3 to 23 nm) than Si-face samples (0.5 to 3.5 nm) grown simultaneously. Transport results were also different between the two faces. The highest 300 K mobilities, obtained for small patterned Hall crosses (2 x 2 or 10 x 10 μm^2, an example is shown in Fig. 1), were for Si-face: 1120 $cm^2 V^{-1} s^{-1}$ for a hole sheet density of 8.5 x 10^{11} cm^{-2}, and for C-face: 18,100 $cm^2 V^{-1} s^{-1}$ for a hole sheet density of 2.1 x 10^{12} cm^{-2}.

For 2-inch SiC substrates, the Si-face orientation was initially chosen for full wafer growth since results suggested better epitaxial thickness control. After growth, wafer-scale variation of resistivity ranged from 11 to 28% for wafers mapped at 300 K by a non-contact Lehighton probe station. The average Lehighton mobility of several wafers ranged from 520 to 2780 $cm^2 V^{-1} s^{-1}$. This result demonstrates that large area graphene epitaxy has similar transport properties as small area samples. Maps of strain and thickness were obtained using Raman spectroscopy (details to be presented by Robinson *et al.* in this conference). In particular, strain was largest at step edges. Non-uniformities in thickness were found to be greatest at these step edges. The wafers were processed to form field effect transistors (FETs) (details to be presented, by Moon *et al.* in this conference). Preliminary FET data demonstrate extrinsic $f_t \cdot L_g$ of 8 GHz·μm with a record f_{max} of 14 GHz at V_{ds} = 5 V. These results make an encouraging argument that large area graphene epitaxy on SiC is technologically viable and makes an excellent choice for the development of graphene-based device technologies.

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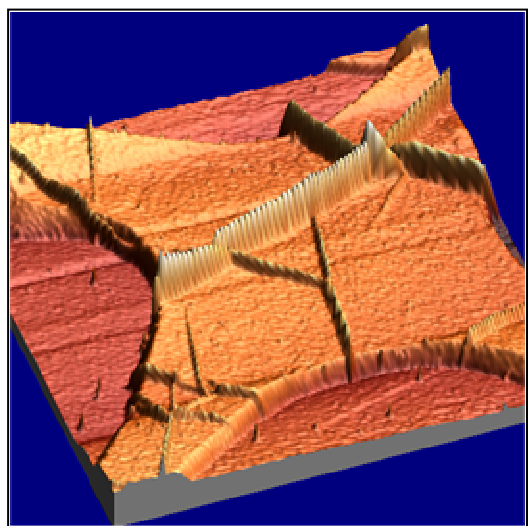

Figure 1 Atomic force microscopy map of a 2 x 2 μm^2 cross having 300 K hole mobility and concentration of 11,600 $cm^2V^{-1}s^{-1}$ and 1.54x10^{13} cm^{-2}, respectively. Note the "giraffe stripe" present in the central region.